GF22: 3.3V Support: Power

AUTOMOTIVE GRADE

Libraries

Name	Process	Form Factor
RGO_GF22_18V33_FDX_25C_SPT	FDX	Staggered CUP
RGO_GF22_18V33_FDX_45C_SPT	FDX	Inline CUP

Summary

The 3.3V Support: Power library provides a full complement of cells to support the assembly of a complete pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

These 22nm libraries are available in inline and staggered CUP wire bond implementations with a flip chip option.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

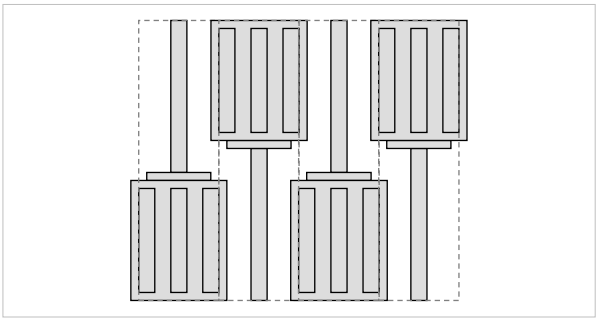
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)
    - 750V corner pin C4B package classification achieved by following key design priorities

Latch-up Immunity:

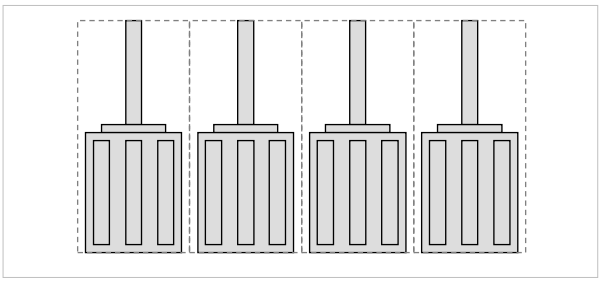
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 30µm x 165µm



Inline (core-limited) – 54µm x 95µm



Cell List

Name	Description
Digital Pads *	
STx_IN_001_1833V_NC	Input-only buffer
I/O Power / Ground Pads *	
PWx_VD_PDO_1833V	I/O power (DVDD) with POC
PWx_VD_RDO_1833V	I/O power (DVDD)
PWx_VS_RDO_1833V	I/O ground (DVSS)
PWx_VS_DRC_1833V	Common ground with I/O ESD
Core Power / Ground Pads *	
PWx_VD_RCD_1033V	Core power (VDD)
PWx_VS_RCD_1033V	Core ground (VSS)
PWx_VS_DRC_1033V	Common ground with Core ESD
Analog Pads *	
ANx_BI_DWR_1833V	1.8V Analog Input cell
ANx_BI_DWR_1033V	0.8V Analog Input cell
Analog Power / Ground Pads *	
PWx_VD_ANA_1033V	Analog power (AVDD) 0.8V
PWx_VS_ANA_1033V	Analog ground (AVSS)
PWx_VD_ANA_1833V	Analog power (ADVDD) 1.8V
PWx_VS_ANA_1833V	Analog ground (ADVSS)
Support Pads	
SPx_CO_000_1833V	Corner cell (rail splitter)
SPx_CO_001_1833V	Corner cell (continuous)
SPx_SP_000_1833V	0.1µm spacer
SPx_SP_001_1833V	1µm spacer
SPx_SP_005_1833V	5µm spacer
SPx_SP_010_1833V	10µm spacer
SPx_RS_005_1833V	Rail splitter
SPx_RE_SVR_182533V *	VREF / HVPS generation
SPx_RE_SVR_1833V *	VREF / HVPS generation
SPx_SP_POC_1833V *	POC generation
SPP_SP_PLS *	POC level shifter

* Vertical-only (_V) and horizontal only(_H) variants provided
Cell names / descriptions abbreviated

Staggered CUP Cells	
CUP_GF22_44X44_IN	44µm X 44µm Inner
CUP_GF22_44X44_OUT	44µm X 44µm Outer
CUP_GF22_FC	Flip chip cell

Inline CUP Cells	
CUP_GF22_44X44_INLINE	44µm X 44µm Inline
CUP_GF22_FC_INLINE	Flip chip cell

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.945	V
		0.72	0.8	0.88	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
		1.35	1.5	1.65	V
		1.08	1.2	1.32	V
T_J	Junction temperature	-40	25	150	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
0.8V (AG2)	FFG	+10%	+10%	-40°C
	FFG	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.9V Overdrive (AG2)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.8V (AG1)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	FFG	+5%	+10%	150°C
	SSG	-10%	-10%	150°C

[1] DVDD = 1.2V, 1.5V, 1.8V, 2.5V & 3.3V

Published by:

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